REMARKS

Summary of the Invention

Claims 25-39 and 47-53 are directed to a "semiconductor component". In the elected embodiment of Figures 1-7, the component can comprise a chip module 24 (Figure 2E), a multi chip module 28 (Figure 3) or a semiconductor package 72 (Figure 7). In each case, the component includes a substrate 10 (Figure 2) and a blanket deposited conductive layer 14 (Figure 2) on the substrate 10. In addition, the component includes conductors 16 (Figure 2) on the substrate 10, and a semiconductor die 20 (Figure 2E, 3A or 7) in electrical communication with the conductors 16. The die 20 can be "flip chip" mounted as shown in Figure 2E, or "wire bonded" as shown in Figure 3A.

Each conductor 16 is defined by a pair of laser machined grooves 15 (Figure 2) in the conductive layer 14. As shown in Figure 2C, the conductors 16 comprise portions of the conductive layer 14 separated by the grooves 15, and by remaining portions of the conductive layer 14. As shown in Figure 2, each conductor 16 includes a bond pad 18 (pads or contacts in the claims) configured for flip chip mounting or wire bonding the die 20. Each conductor 16 can also include a contact pad 22 (contacts in the claims) configured for electrical connection to outside circuitry. In the case of wire bonding, an opening 40 (Figure 3A) can be laser machined in the conductive layer 14 for attaching the die 20 to the substrate.

As shown in Figure 5A, the substrate 10BGA can also include conductive vias 58 in electrical communication with the conductors 16BGA, and contact balls 66 in electrical communication with the conductive vias 58.

Claim Rejections Under 35 USC 103(a)

Claims 25-29 and 47-53 have been rejected under 35 USC 103(a) as being unpatentable over Hembree et al. (US Patent

No. 5,783,461) in view of Frankeny et al. (US Patent No. 5,065,227), Pedder (US Patent No. 5,717,245) and Gilmour et al. (US Patent No. 5,391,917).

The rejections under 35 USC §103 are traversed for the reasons to follow. In the alternative, the rejections under 35 USC §103 are submitted to have been overcome by the amendments to the claims. Specifically, each of the independent claims has been amended to recite a component having a substrate and a "blanket deposited conductive layer" on or covering the substrate. Antecedent basis for the additional recitations is contained on page 3, lines 9-10, and on page 7, lines 8-9 of the specification. The additional recitations have been added to further distinguish the presently claimed semiconductor component from the prior art.

In order to establish a prima facie case of obviousness under 35 USC §103 a combination of references must teach or suggest all the claim limitations (MPEP 2142, 2143). However, the cited combination of references does not teach a blanket deposited conductive layer having a pattern of conductors defined by laser machined grooves through the conductive layer.

The primary reference to Hembree describes a temporary semiconductor package for testing semiconductor dice. The package 10 (Figure 1) includes an interconnect 16 having raised contact members 60 (Figure 4) for making electrical connections with bond pads 62 on the die 12 (column 6, lines 27-30). In addition, the interconnect 16 includes conductive layers 68 (Figure 5) on the contact members 60, and conductive traces 58 (Figure 4) in electrical communication with the conductive layers 68 (column 6, lines 37-40). Although the conductive traces 58 perform the same function as the presently claimed conductors (i.e., signal transmission), the conductive traces 58 are not defined by laser machined grooves through a blanket deposited conductive layer.

In support of the rejections the Office Action states that Hembree discloses "each conductor comprising a plurality of first grooves/raised contact members (40/68/70, etc. in Fig. 2-5A) through the conductive layer". This interpretation is incorrect, as the conductive layers 68 cover the contact members 60 and do not form the conductive traces 58. Further, there are no grooves through the conductive layers 68, and the raised contact members 60 could not possibly be considered grooves through the conductive layers 68.

Pedder also does not disclose or suggest conductors defined by laser machined grooves through a blanket deposited conductive layer. Pedder discloses a BGA device having a multilayered substrate 12 that includes microstrip trimming stubs 94, 95 which are trimmed using a laser (column 8, lines 46-54). However, the trimming stubs 94, 95 are formed using a conventional metallization process (column 4, lines 11-18), and are then trimmed to a desired length using a laser to achieve electrical tuning (column 6, lines 60-63). Although the length of the trimming stubs 94, 95 is adjusted by laser trimming, the trimming stubs 94, 95 are not defined by laser machined grooves in a blanket deposited conductive layer. Rather, the grooves which define the trimming stubs 94, 95 are already present, and the laser merely removes a portion of the stubs 94, 95.

Gilmour et al. also does not disclose or suggest conductors formed by laser machined grooves in a blanket deposited conductive layer. Rather, Gilmour et al. was cited as teaching laser machined vias having a spacing of 40 μm. In contrast, with the present invention the laser machined grooves can be as small as about 5 μm, such that the conductors also have a spacing of only about 5 μm. The prior art vias thus having a spacing eight times greater than the spacing of the present conductors. Rather than supporting an obviousness rejection, Gilmour et al. would tend to demonstrate the unobviouness of the present claims.

Frankeny et al. also does not disclose or suggest conductors formed by laser machined grooves in a blanket deposited conductive layer. Rather, Frankeny et al. teaches "a laser drilling operation" at column 5, line 65 to form a conductive via. However, the copper layer (i.e., conductors) in Figure 5 of Frankeny et al. is formed using "traditional plating, photoimaging, and etching techniques common to printed wiring board manufacture."

In support of the 35 USC §103 rejections the Office Action states "Frankeny et al. further teach forming the conductors comprising portions of the conductive layer electrically isolated from one another by the grooves and separated by remaining portions of the conductive layer where the conducting layer is patterned using conventional plating and etching methods". This statement is incorrect, as the lasered conductive vias in Frankeny et al. do not form grooves which electrically isolate the conductors. Rather the lasered conductive vias electrically connect the conductors. Further, with conventional plating and etching methods no portions of the conductive layer remain to separate the conductors, as only the conductors remain.

In addition to the primary feature of conductors formed by laser machined grooves in a blanket deposited conductive layer, claims 25, 32 and 52 also recite "conductive vias" in electrical communication with the conductors. Further, claims 34 and 35 recite "an encapsulant" on the die. Still further, claims 37 and 47 recite "pads" or "contacts" on the conductors, which are also defined by the laser machined grooves. These features in combination with conductors having the presently claimed structure, are submitted to define unobvious subject matter.

In addition to not disclosing all of the presently claimed features, Applicants submit there is no incentive for the proposed combination of references as required by MPEP 2142, 2143. As support for the combination of

references the Office Action states: "Therefore it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a plurality of conductors defined by a plurality of laser machined first or second grooves through the conductive layer, the conductors comprising portions of the conductive layer electrically isolated from one another by the grooves and separated by remaining portions of the conductor layer, the grooves having a width as small as 5 microns so that the resonance characteristics and electrical performance of the contacts/device can be improved using Pedder, Gilmour et al. and Frankeny et al's conductor structure in Hembree's component."

However, Applicants submit that the above statement is incorrect, as Pedder, Gilmour et al. and Frankeny et al. do not suggest conductors formed by laser machined grooves in a blanket deposited conductive layer. In addition, the proposed combination of references appears to be based on a hindsight reading of the present disclosure, rather than on an objective analysis of the prior art. In this regard, the Examiner is requested to assess unobviousness from the viewpoint of one skilled in the art at the time of the invention, and without the benefit of the present disclosure.

As stated in W.L. Gore & Associates V. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Nov. 14, 1983):

"To imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used against its teacher."

When viewed in the correct context the present claims "taken as a whole" are submitted to be unobvious over the art.

Conclusion

In view of the above amendments and arguments, favorable consideration and allowance of claims 25-39 and 47-53 is requested. Should any issues remain, the Examiner is asked to contact the undersigned by telephone.

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October 4, 2002
Date of Signature

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Marked Version Of Claims Showing Changes

25. (four times amended) A semiconductor component comprising:

a substrate having a first surface and an opposing second surface;

a blanket deposited conductive layer on the first surface;

a plurality of conductors on the first surface defined by a plurality of laser machined grooves through the conductive layer to the substrate, the conductors comprising portions of the conductive layer electrically isolated by the grooves and separated by remaining portions of the conductive layer;

[, the conductors and the grooves having a width as small as about 5 μm;]

at least one semiconductor die on the [first surface] substrate in electrical communication with the conductors;

a plurality of conductive vias in the substrate from the first surface to the second surface in electrical communication with the conductors; and

a plurality of external contacts on the second surface in electrical communication with the conductive vias.

30. (four times amended) A semiconductor component comprising:

a substrate having a surface;

a blanket deposited conductive layer [on] substantially covering the surface and having a thickness;

a plurality of conductors and pads on the surface defined by a plurality [of pairs] of laser machined grooves through the thickness of the conductive layer to the substrate extending on the surface in a [first direction and in a second] plurality of directions, each conductor and each pad comprising a portion of the conductive layer electrically isolated by [a plurality of] at least one pair of laser machined grooves; and

a semiconductor die flip chip mounted or wire bonded to the pads.

35. (four times amended) A semiconductor component comprising:

a substrate having a surface;

a blanket deposited conductive layer on the surface;

a plurality of conductors on the surface comprising portions of the conductive layer, the conductors defined and electrically isolated by a plurality of laser machined grooves through the conductive layer to the substrate, each conductor defined by at least one pair of laser machined grooves;

[having a width and each groove having a spacing as small as about 5μm; and]

a semiconductor die on the substrate in electrical communication with the conductors; and

an encapsulant on the substrate covering the die and the conductive layer.

36. (thrice amended) The semiconductor component of claim 35 wherein the die is flip chip mounted or wire bonded to the conductors.

[further comprising an encapsulant at least partially covering the semiconductor die and at least a portion of the surface.]

47. (four times amended) A semiconductor component comprising:

a substrate having a surface;

a blanket deposited conductive layer [on] substantially covering the surface; and

a plurality of conductors on the surface defined by a plurality of laser machined grooves through the conductive layer to the surface and extending in a [first direction or a second] plurality of directions on the surface, the

conductors comprising portions of the conductive layer which are electrically [insulated] isolated from one another by the laser machined grooves, the portions of the conductive layer including first contacts on first ends thereof configured for bonding, and second contacts on second ends thereof configured for electrical connection to external circuitry; and

a semiconductor die on the substrate bonded to the first contacts.

52. (thrice amended) A semiconductor component comprising:

a substrate having a surface;

a blanket deposited conductive layer on the surface;

a plurality of conductors on the surface defined by a plurality of first laser machined grooves through the conductive layer to the surface, the conductors comprising portions of the conductive layer electrically isolated by the grooves and separated by remaining portions of the conductive layer;

a plurality of contacts on the conductors defined by a plurality of second laser machined grooves through the conductive layer to the surface;

a plurality of conductive vias through the substrate in electrical communication with the conductors; and

a semiconductor die on the substrate in electrical communication with the contacts.